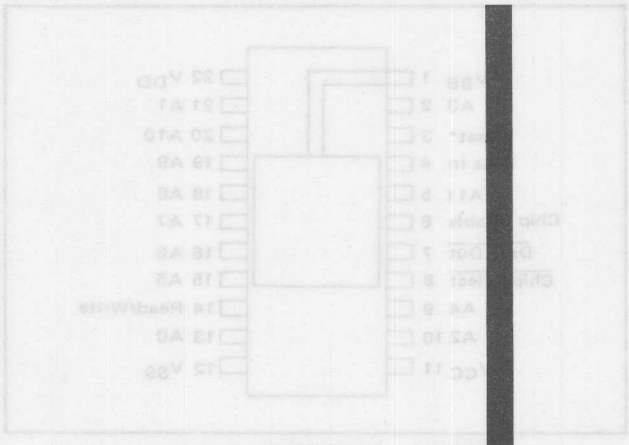
AN-740
Application Note

THE DESIGN OF AN N-CHANNEL 16K X 16 BIT MEMORY SYSTEM FOR THE PDP-11



Prepared by
Dick Brunner
Computer Applications Engineering

This application note describes the design and construction of a main-frame memory system with MCM6605 N-Channel MOS memories. Topics included are: the interface to the PDP-11, refresh control and bookkeeping, timing control logic for the memories, memory system considerations, and organization. The memory also features new integrated circuits that reduce package count and enhance memory system performance.

MOTOROLA Semiconductor Products Inc.

THE DESIGN OF AN N-CHANNEL 16K X 16 BIT MEMORY SYSTEM FOR THE PDP-11

INTRODUCTION

When PMOS dynamic random access memories were introduced, they offered, for the first time, memory systems with a cost/performance exceeding that of cores. Although they have been fairly successful in competing with core memories for mainframe applications, there were many shortcomings. For example, some memories required critical overlapping clock pulses which complicated the design and placed an extreme burden on the layout. The logic levels for both input and output were not compatible with standard logic, such as TTL, which meant that translators had to be used. The actual cost of these translators is small compared to the penalty paid for the added complexity of the memory board, additional power, and extended system cycle time. Also additional bypassing is required and the board layout complicated by the ac noise generated from the translators.

With the advent of N-channel and advanced design techniques, a whole new breed of MOS memories has emerged. One such memory is the MCM6605. The MCM6605 is a 4096-word by 1-bit dynamic memory that does not exhibit any of the undesirable features mentioned earlier. For example: This memory requires only one clock that has no critical overlaps. All inputs and outputs are TTL compatible, and the memory access time is fast (210 ns max). Other features include chip select for easy memory expansion and three-state output. Because of the high density, low power, and high speed of this semiconductor memory, it is ideal for mainframe memory applications.

This paper briefly covers the operation and features of the MCM6605, and then illustrates the design of a PDP-11 add-on mainframe memory system employing the MCM6605. The memory system to be described contains 16K words by 16 bits or 32K bytes of semiconductor memory and the associated electronics necessary to control and interface the semiconductor memory to the PDP-11. The whole memory system can be mounted on a single P.C. board because of the small amount of support electronics required and the high density of the MCM6605 memory.

The support electronics can be easily partitioned into three sections or functions: bus interface, refresh timing and control, and memory control and interface. A detailed description is given of the logic and interface devices necessary to perform each of these functions.

The paper is concluded with a summary on the performance of this add-on memory system with the PDP-11 computer.

MCM6605 OPERATION

The MCM6605 is a dynamic random access memory that contains 4096 bits of storage organized into 4096 words by 1 bit. This semiconductor memory, which comes in a standard 22-pin package, see Figure 1, is fabricated with an N-channel silicon gate process to optimize speed, power, and density tradeoffs. By employing the standard three transistor cell arrangement, the internal sense amplifier requirements were simplified.

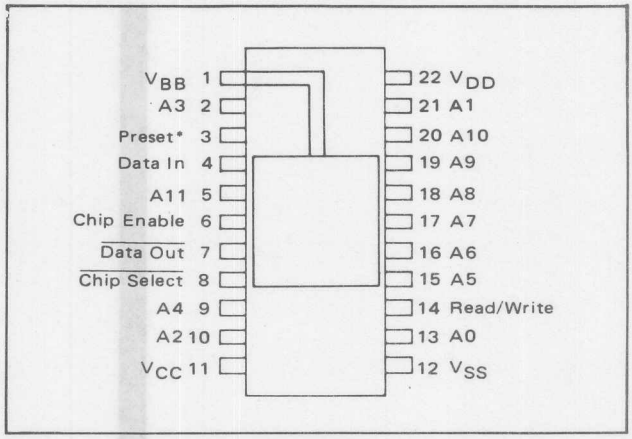


FIGURE 1 – MCM6605 Pin Assignment

In addition to the high speed (210 ns access) and low power (82 μW/bit active and 0.63 μW/bit standby), the MCM6605 has additional features such as TTL-compatible inputs with latch capability on the address inputs, three-state output with chip select control for easy memory expansion in the word direction, only 32 refresh cycles required every 2 ms, and the power supply pins on the corner of the package to simplify power supply distribution and bypassing on the board. One high-voltage clock is required and there is no critical timing or signal overlap.

The net result of these features can provide a big saving in system costs, not only because of the lower cost of the semiconductor memory per bit, but because of the increased packaging density per board, less support electronics, bipolar logic compatibility, reduced power, and lower assembly costs. All of these savings will be apparent in the memory system to be covered in the following sections.

A detailed description of the operation of the MCM6605 is necessary for the design of the memory controller. The 4096 bits of storage are divided equally into four quad-

rants as noted in the block diagram given in Figure 2. In addition to the storage, the chip contains input address latches, row and column decoder logic plus additional logic to control the input and output of data to the storage area.

The MCM6605 uses three internal clock signals to control reading from, or writing into, the storage cells. These three clock signals ($\phi1$, $\phi2$, and $\phi3$ shown in Figure 2) are controlled by Chip Enable (CE) and Read/Write (R/W) to perform the various read, write, refresh, or combination cycles possible with the MCM6605. The timing for these cycles is given in Figures 3 and 4.

The $\phi1$ clock is on whenever CE is low (standby position) and precharges the dynamic circuitry of the MCM6605 in preparation for the start of a memory cycle.

Read Cycle

The one high level clock line, CE, is brought high to initiate all cycles. The rising edge of CE turns off the $\phi1$ precharge and initiates the $\phi2$ clock. The $\phi2$ clock does several things in sequence. First, it latches the input addresses into buffers and drives the column decoders. These decoders use addresses A0 to A4 to select one column of 64 storage cells on each side of the chip and transfer the 128 stored data bits onto precharged bit sense lines. The row decoders use A5 to A11 to select one bit of the 128 bit sense lines. This selected bit is exclusive NORed with a data control cell (the purpose of which is explained under write cycle below) and is used to drive an output buffer/latch. The $\phi2$ signal terminates at this time after latching the data into the output buffer. The cycle can be terminated at this point by bringing CE low to standby, allowing $\phi1$ to precharge the memory before the next cycle. During this simple read cycle, R/W must remain high to inhibit writing.

Write Cycle

The write cycle is the same as a read cycle, up until $\phi2$ terminates with 128 bit sense lines holding the two columns of data. When $\phi2$ goes off, a $\phi3$ signal is initiated anytime R/W is in the write position. This $\phi3$ clock transfers the data on the 128 bit sense lines back into the storage array. The line selected by the row decoder (A5 – A11), however, has been overridden by input data. The write cycle is terminated by bringing CE low into standby. The $\phi2$ – $\phi3$ sequence of bringing data from the

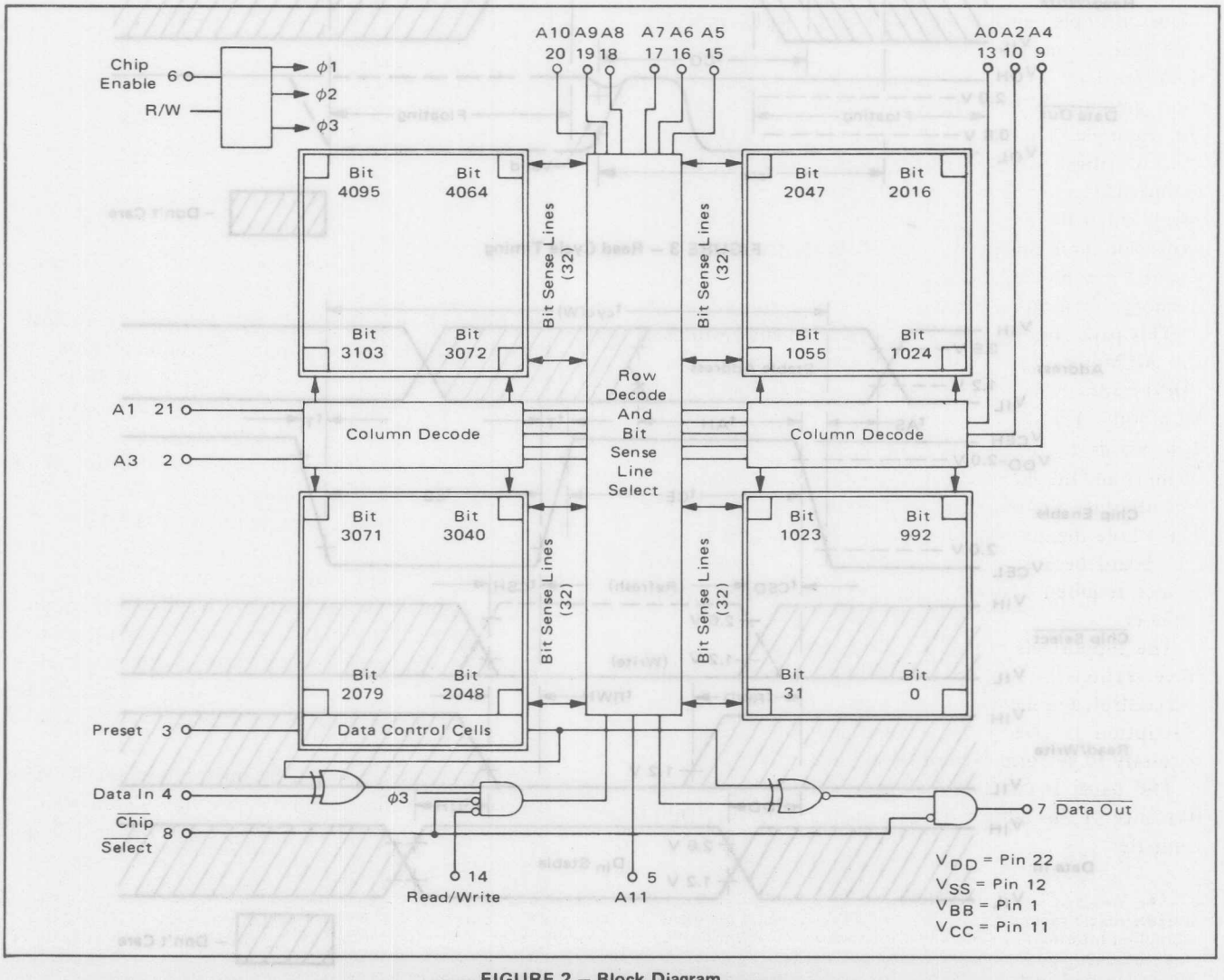


FIGURE 2 – Block Diagram

storage cells onto bit sense lines and then putting the data back into the cells inverts the stored data since the read operation is inverting but the write operation is not. In order to keep track of the polarity of the stored data, a row of data control cells is added to the array and is driven by the same column decoder which drives the storage cells. The data control cells are identical to the storage cells and are inverted each time a write cycle is performed. By performing an exclusive NOR function of both input and output data with the control cell tied to the same column, the relative polarity is always discernable and inversions do not cause loss of data.

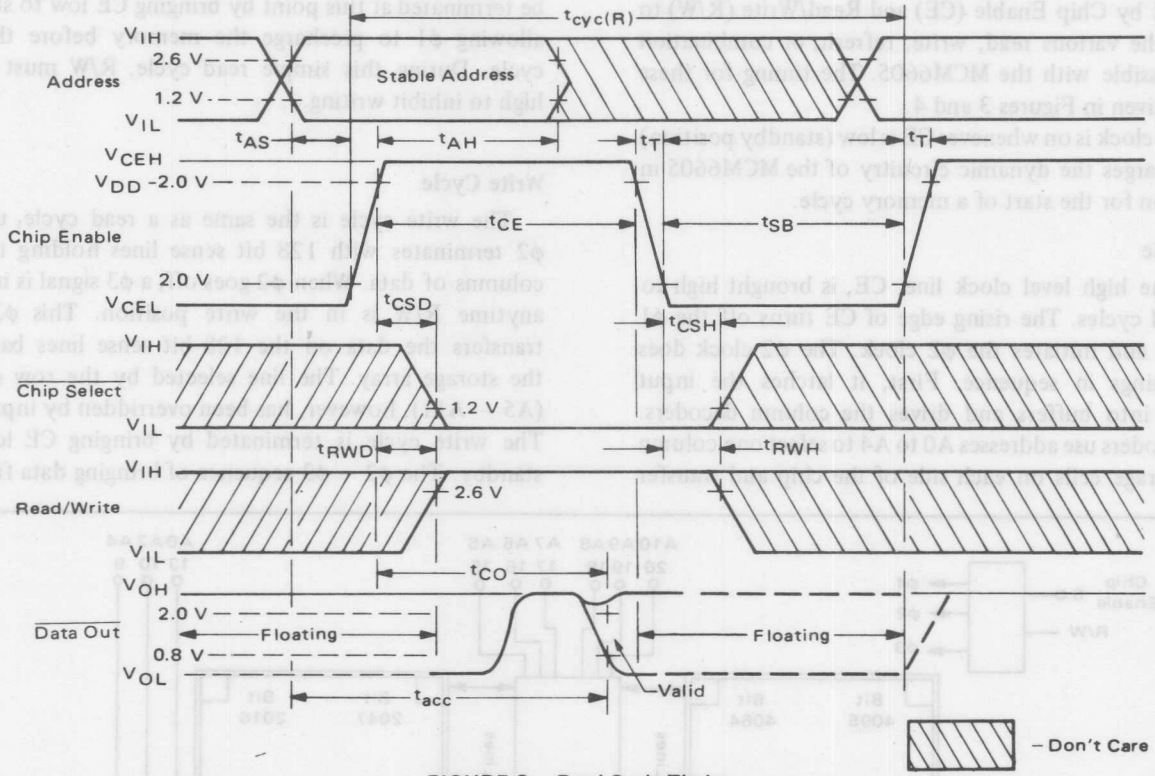


FIGURE 3 – Read Cycle Timing

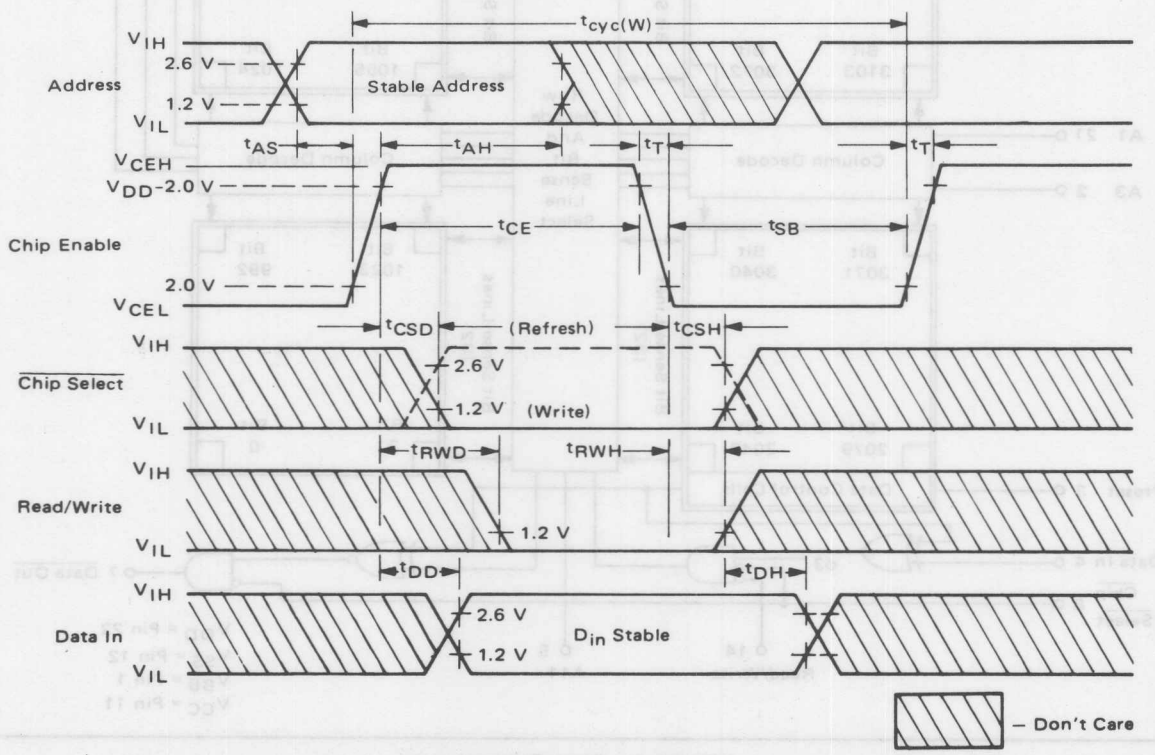


FIGURE 4 – Write and Refresh Cycle Timing

Refresh Cycle

The write operation described above actually refreshes 127 bits in the selected columns while it is writing into one bit. If the Chip Select ($\overline{CS}$) signal is held high to inhibit the input data, then a write cycle would merely refresh all 128 bits. Therefore, one write cycle with $\overline{CS}$ high (now called a refresh cycle) on each of the 32 combinations of A0 through A4 will refresh the entire memory as long as each address combination is used every 2 ms.

When the memory is first powered up, the data control cells may not come up with a valid logic level and several refresh cycles may be required to insure a solid logic level. In system usage, this would cause no difficulty, since data would not normally be immediately written into the memory system. For memory test purposes, a preset input (pin 3) is included to preset these data control cells with a 200 ns pulse. This preset pin should be permanently grounded in systems unless there is some unusual requirement.

Keeping the above memory operation in mind, the first phase of the design will be the PDP-11 interface.

MEMORY SYSTEM

First of all, the memory system can be divided into four distinct functions or sections as illustrated in Figure 5: the memory – CPU interface, refresh address and control, memory timing control, and the memory array.

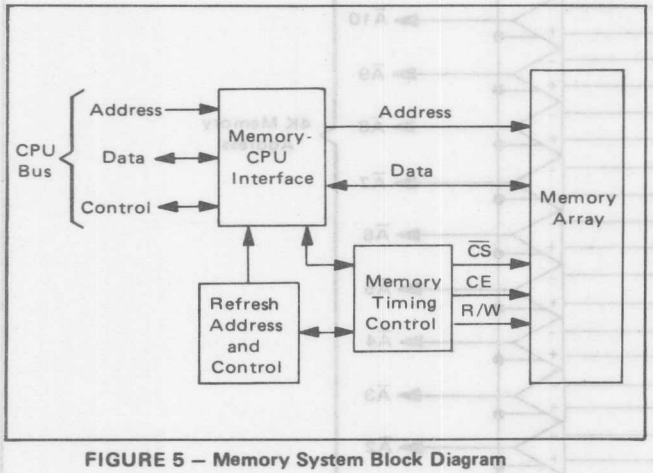


FIGURE 5 – Memory System Block Diagram

1. Memory – CPU Interface

To interface with the PDP-11 computer, the following bus lines are required: 18 address, 16 data, and 4 control. The least significant address bit, $\overline{A}00$, is actually used with the control bits C0 and C1 to determine if a write cycle is to be done on the lower byte (data bits D0 – D7) or upper byte (data bits D8 – D15) as illustrated in Figure 6. The next 12 address bits, $\overline{A}1$ through $\overline{A}12$, go directly to the memories to select one word from 4096 words; see Figure 7. Address bits $\overline{A}13$ and $\overline{A}14$ are used to select one 4K memory block from the 16K words per memory board.

Address bits $\overline{A}15$, $\overline{A}16$ and $\overline{A}17$ permit the main-memory capacity of the PDP-11 to be expanded to 128K words. Thus, only eight 16K memory boards are required for the complete main-memory capacity of the PDP-11. The jumper box, illustrated in Figure 7, can be wired to decode address bits $\overline{A}15$, $\overline{A}16$ and $\overline{A}17$ for the selection of only one of the eight memory boards.

C0	C1	$\overline{A}00$	Condition
X	0	X	Read
0	1	X	Write (0-15)
1	1	0	Write (0-7)
1	1	1	Write (8-15)

X = Don't Care

FIGURE 6 – Memory Control Truth Table (PDP-11)

The bus lines require special circuits to receive and transmit data so that the transmission-line characteristics of the lines will be maintained. The circuits chosen for this job were the MC3450/MC3452 quad line receivers and the MC4042 quad pre-driver.

The MC3450/MC3452 Bus Receiver

The MC3459 is a quad receiver that features three-state outputs; the MC3452 has open collector outputs. These line receivers were chosen because of the following features:

(1) High input impedance keeps loading of the line to a minimum.
(2) Minimum overdrive to switch receiver is 25 mW, which provides high noise immunity.
(3) The differential input amplifier stage of the receiver can be used to provide either true or complement signals; see Figure 7.
(4) Four receivers per package greatly reduce the total package count.

In order to use the MC3450 or MC3452 as a single-ended line receiver, one input to the differential receiver has to be tied to a reference voltage. For optimum noise immunity, the reference voltage should be set halfway between the minimum high and maximum low voltage specified for the line. Minimum high for this system is 2.5 V and maximum low is 1.4 V. The optimum reference voltage (V_{ref}) for these limits would be 1.95 V. The reference voltage generator is given in Figure 7. The voltage generator is designed to give a constant V_{ref} of 1.95 V regardless of the line receiver current drain. The 1N914 diode is used to track the base-emitter voltage of the 2N3904 with temperature, thus providing relatively constant output voltage over temperature. Note that true and complement signals (A00/$\overline{A}$00) in Figure 7 are easily generated by attaching the V_{ref} voltage to either the non-inverting or inverting inputs respectively.

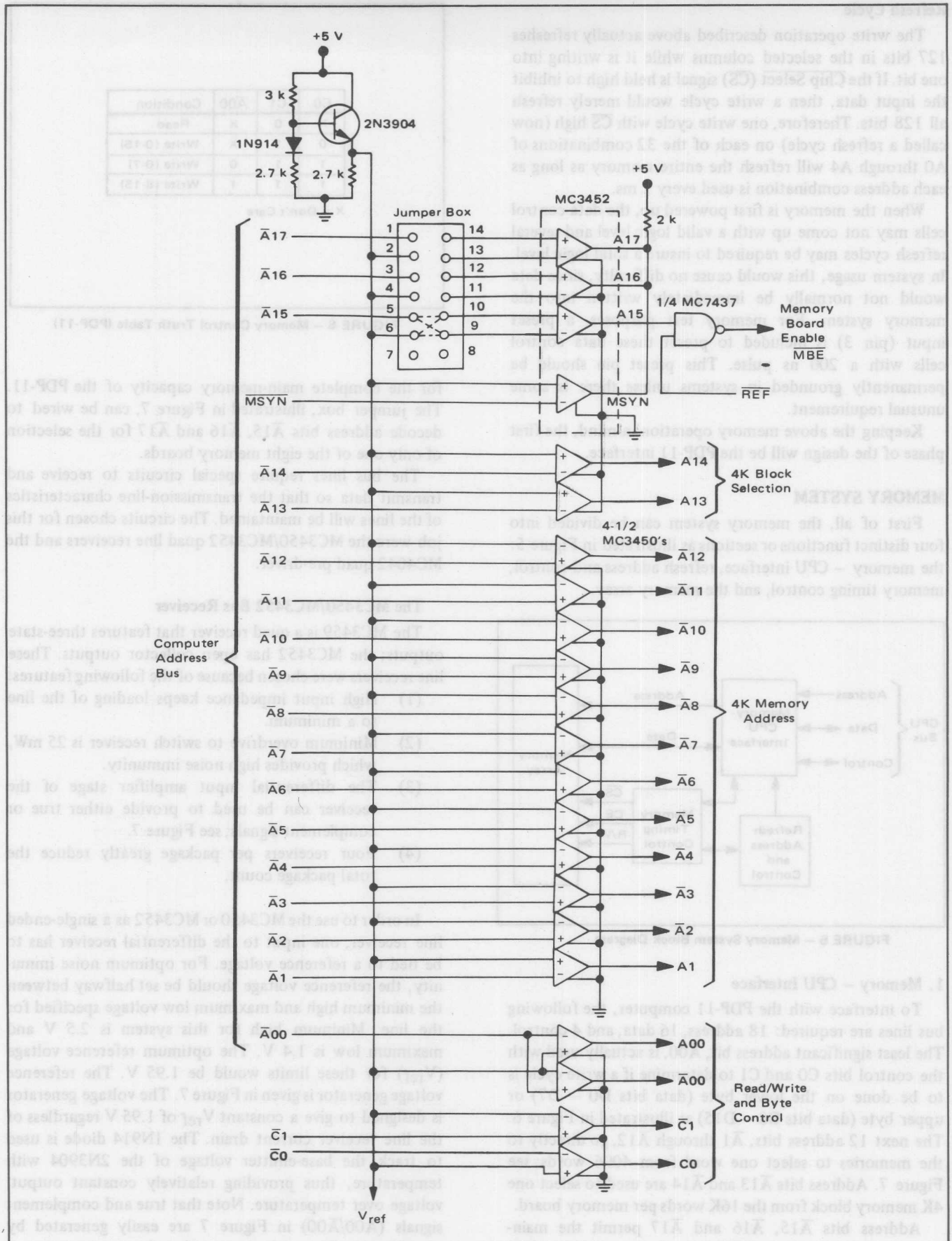


FIGURE 7 – CPU/Memory Address and Control Interfaces

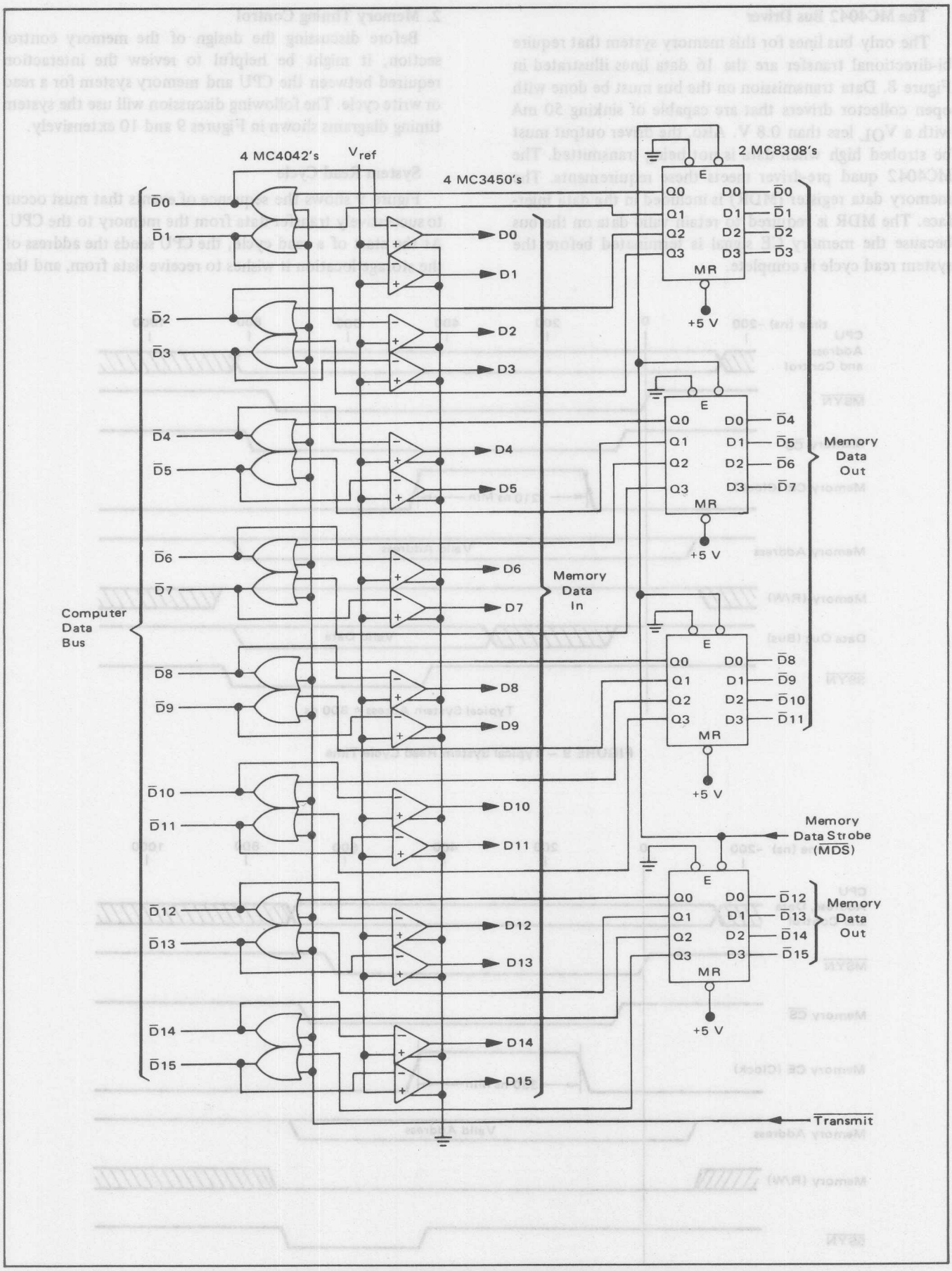


FIGURE 8 – CPU/Memory Data Interface

The MC4042 Bus Driver

The only bus lines for this memory system that require bi-directional transfer are the 16 data lines illustrated in Figure 8. Data transmission on the bus must be done with open collector drivers that are capable of sinking 50 mA with a V_{OL} less than 0.8 V. Also, the driver output must be strobed high when data is not being transmitted. The MC4042 quad pre-driver meets these requirements. The memory data register (MDR) is included in the data interface. The MDR is required to retain valid data on the bus because the memory CE signal is terminated before the system read cycle is complete.

2. Memory Timing Control

Before discussing the design of the memory control section, it might be helpful to review the interaction required between the CPU and memory system for a read or write cycle. The following discussion will use the system timing diagrams shown in Figures 9 and 10 extensively.

System Read Cycle

Figure 9 shows the sequence of events that must occur to successively transfer data from the memory to the CPU. At the start of a read cycle, the CPU sends the address of the storage location it wishes to receive data from, and the

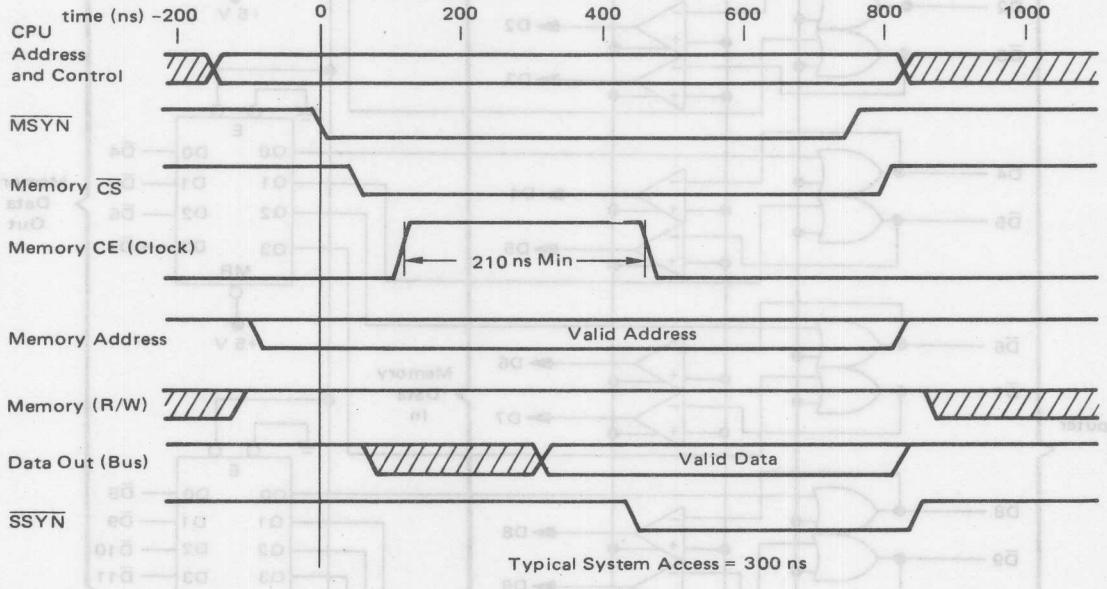


FIGURE 9 – Typical System Read Cycle Time

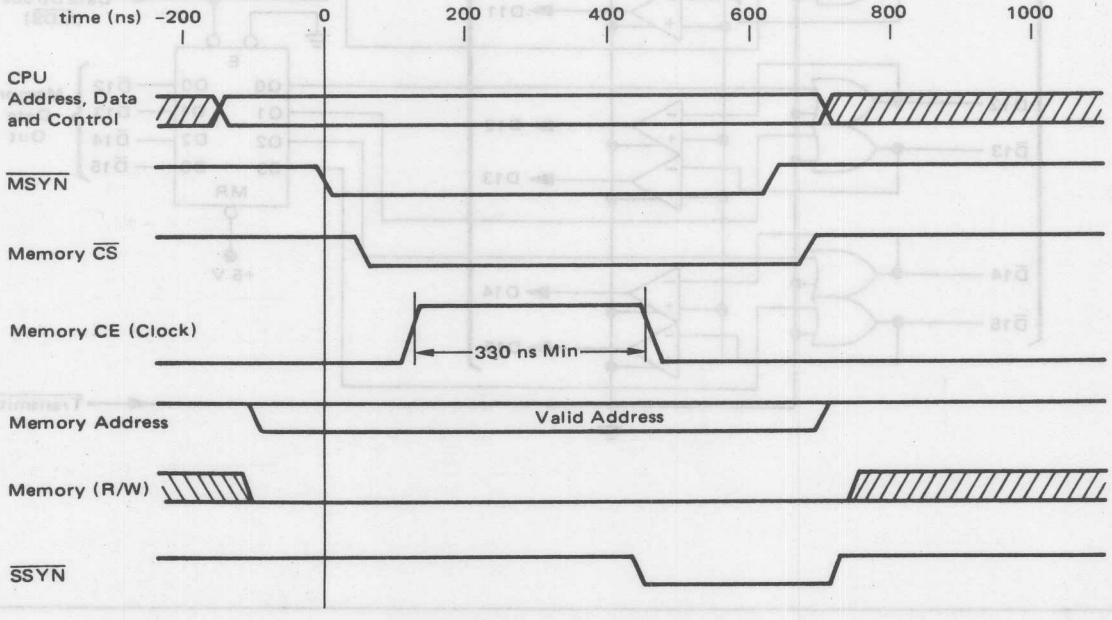


FIGURE 10 – Typical System Write Cycle Time

control lines ($\overline{C0}$, $\overline{C1}$) tell the memory system that the operation to be performed is a read cycle. The logic state of $\overline{C0}$ and $\overline{C1}$ for a read cycle is given in Figure 6. The CPU waits for at least 150 ns to allow for address deskewing and decoding before signaling the start of a read cycle with a master synchronization signal ($\overline{MSYN}$). The remaining signals shown in Figure 9, with the exception of the slave synchronization signal ($\overline{SSYN}$), are the same as those given in Figure 3. When the control board receives $\overline{MSYN}$, the $\overline{CS}$ and CE signals are sent to the memories. At the end of the 210 ns Chip Enable clock, the memory controller must generate $\overline{SSYN}$ to indicate that the data read from the memories is valid. When $\overline{SSYN}$ is sent, the CPU strobes in the data and terminates the cycle by releasing $\overline{MSYN}$.

System Write Cycle

With a write cycle, the data and the address of where the data is to be stored are placed on the bus as indicated in Figure 10. The logic states of $\overline{C0}$, $\overline{C1}$, and $\overline{A00}$ (Figure 6) determine whether the write cycle to be performed is a byte or a word. As with the read cycle, 150 ns is allowed for deskewing and decoding before $\overline{MSYN}$ is sent. The remaining signals given in Figure 10 are the same as those given in Figure 4. When the memory board receives $\overline{MSYN}$, the data, $\overline{CS}$, and CE signals are sent to the memories. At the end of the 330 ns Chip Enable pulse, the memory controller sends $\overline{SSYN}$ to the CPU to signal that the data has been stored. The CPU then terminates the write cycle by releasing $\overline{MSYN}$.

It should be apparent from the preceding discussion that the timing required for either a read or write cycle is extremely simple and that no critical overlapping of signals is required. The complete memory control section is given in Figure 11. Keeping the above memory timing description in mind, the memory control section performs in the following manner.

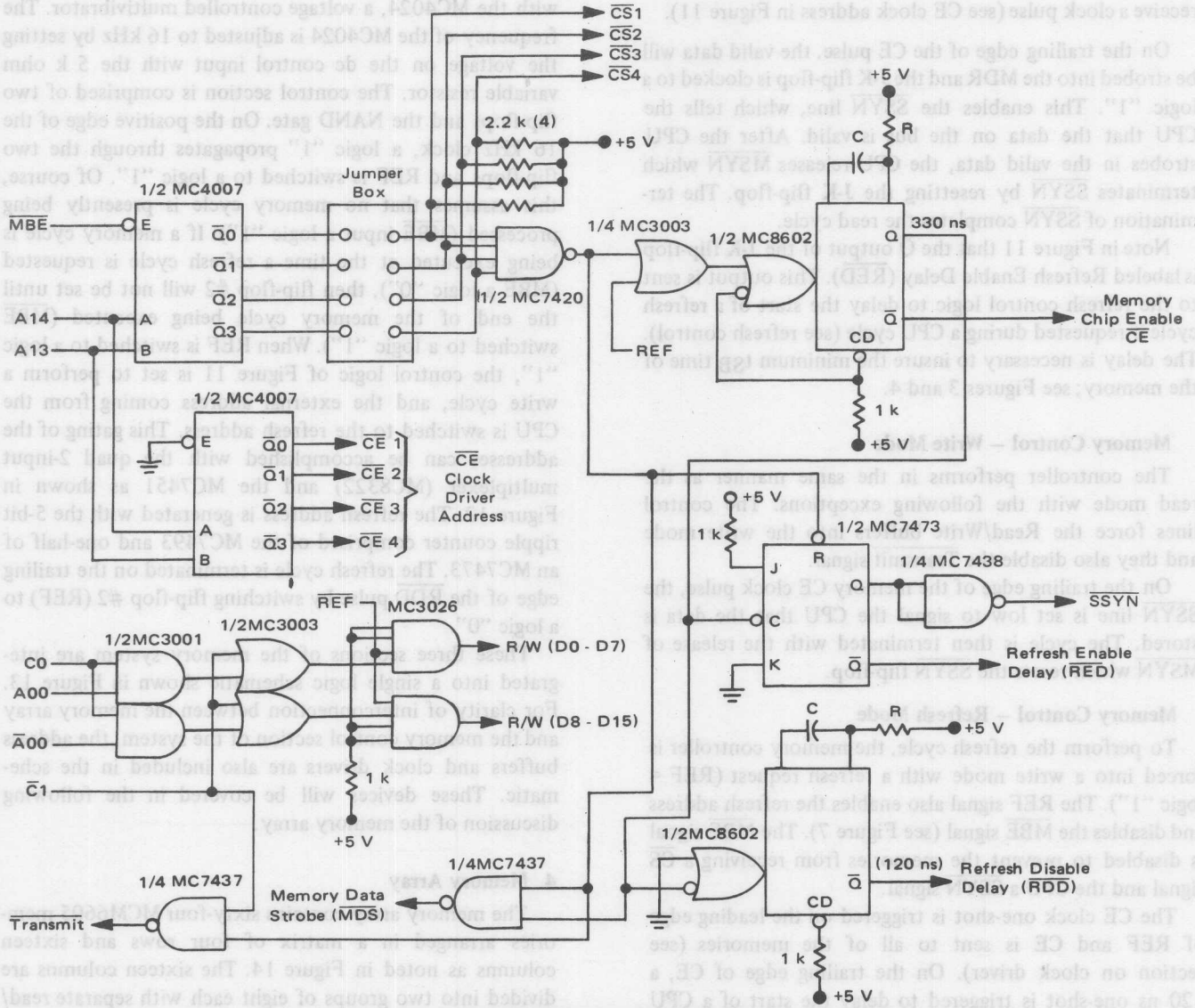


FIGURE 11 – Memory Control Section

Memory Control – Read Mode

Although the CE clock time of the MCM6605 for a read cycle is 120 ns less than that for a write cycle, the CE time for both the read and write cycles was made equal to simplify the memory controller.

For the read cycle, the logic states of control lines C0 and C1 force the read/write buffers into the logic "1" state. A memory board enable ($\overline{MBE}$) signal is generated from the memory – CPU interface circuitry (Figure 7) when the $\overline{MSYN}$ line goes low with the presence of a valid memory board address. The $\overline{MBE}$ signal propagates through the one-of-four demultiplexer (MC4007) and a $\overline{CS}$ signal is sent to the row of memories determined by addresses A13 and A14. The jumper box allows the memory board to be only partially populated for smaller size memory requirements.

The $\overline{CS}$ signal also enables the data bus drivers with $\overline{Transmit}$, and the leading edge of $\overline{CS}$ triggers the MC8602 one-shot which sets the memory CE clock pulse width (330 ns min). To conserve power, the memory CE clock driver is decoded so that only one row of memories will receive a clock pulse (see CE clock address in Figure 11).

On the trailing edge of the CE pulse, the valid data will be strobed into the MDR and the J-K flip-flop is clocked to a logic "1". This enables the $\overline{SSYN}$ line, which tells the CPU that the data on the bus is valid. After the CPU strobes in the valid data, the CPU releases $\overline{MSYN}$ which terminates $\overline{SSYN}$ by resetting the J-K flip-flop. The termination of $\overline{SSYN}$ completes the read cycle.

Note in Figure 11 that the $\overline{Q}$ output of the J-K flip-flop is labeled Refresh Enable Delay ($\overline{RED}$). This output is sent to the refresh control logic to delay the start of a refresh cycle if requested during a CPU cycle (see refresh control). The delay is necessary to insure the minimum t_{SB} time of the memory; see Figures 3 and 4.

Memory Control – Write Mode

The controller performs in the same manner as the read mode with the following exceptions. The control lines force the Read/Write buffers into the write mode and they also disable the $\overline{Transmit}$ signal.

On the trailing edge of the memory CE clock pulse, the $\overline{SSYN}$ line is set low to signal the CPU that the data is stored. The cycle is then terminated with the release of $\overline{MSYN}$ which resets the $\overline{SSYN}$ flip-flop.

Memory Control – Refresh Mode

To perform the refresh cycle, the memory controller is forced into a write mode with a refresh request (REF = logic "1"). The REF signal also enables the refresh address and disables the $\overline{MBE}$ signal (see Figure 7). The $\overline{MBE}$ signal is disabled to prevent the memories from receiving a $\overline{CS}$ signal and the CPU a $\overline{SSYN}$ signal.

The CE clock one-shot is triggered on the leading edge of REF and CE is sent to all of the memories (see section on clock driver). On the trailing edge of CE, a 120 ns one-shot is triggered to delay the start of a CPU cycle that could be requested during a refresh cycle. This signal insures the minimum t_{SB} time of the memory by keeping the $\overline{MBE}$ signal disabled for at least 120 ns after the trailing edge of CE (see refresh control).

3. Refresh Address and Control

In order to insure that data is retained, the whole memory must be completely refreshed every 2 ms as noted earlier. This can be accomplished by insuring that a write cycle is performed on each of the 32 column addresses at least once every 2 ms. There are two ways in which refresh can be performed. One method would be to initiate at the end of a 2 ms period a burst of 32 column refreshes, one refresh cycle followed immediately by another. The second would be to steal one column refresh cycle every 62.4 μs. The latter approach was taken since it would present the least interference to programs being executed by the CPU.

To implement refresh, the following logic is needed: a 16 kHz clock, one 3-input NAND gate, two D latches, a 5-bit ripple counter, and a 5-channel digital multiplexer as illustrated in Figure 12. The 16 kHz can be generated with the MC4024, a voltage controlled multivibrator. The frequency of the MC4024 is adjusted to 16 kHz by setting the voltage on the dc control input with the 5 k ohm variable resistor. The control section is comprised of two flip-flops and the NAND gate. On the positive edge of the 16 kHz clock, a logic "1" propagates through the two flip-flops and REF is switched to a logic "1". Of course, this assumes that no memory cycle is presently being processed ($\overline{MBE}$ input a logic "1"). If a memory cycle is being executed at the time a refresh cycle is requested ($\overline{MBE}$ a logic "0"), then flip-flop #2 will not be set until the end of the memory cycle being executed ($\overline{MBE}$ switched to a logic "1"). When REF is switched to a logic "1", the control logic of Figure 11 is set to perform a write cycle, and the external address coming from the CPU is switched to the refresh address. This gating of the addresses can be accomplished with the quad 2-input multiplexer (MC8322) and the MC7451 as shown in Figure 12. The refresh address is generated with the 5-bit ripple counter comprised of the MC7493 and one-half of an MC7473. The refresh cycle is terminated on the trailing edge of the $\overline{RDD}$ pulse by switching flip-flop #2 (REF) to a logic "0".

These three sections of the memory system are integrated into a single logic schematic shown in Figure 13. For clarity of interconnection between the memory array and the memory control section of the system, the address buffers and clock drivers are also included in the schematic. These devices will be covered in the following discussion of the memory array.

4. Memory Array

The memory array contains sixty-four MCM6605 memories arranged in a matrix of four rows and sixteen columns as noted in Figure 14. The sixteen columns are divided into two groups of eight each with separate read/write control signals. This partitioning scheme provides for

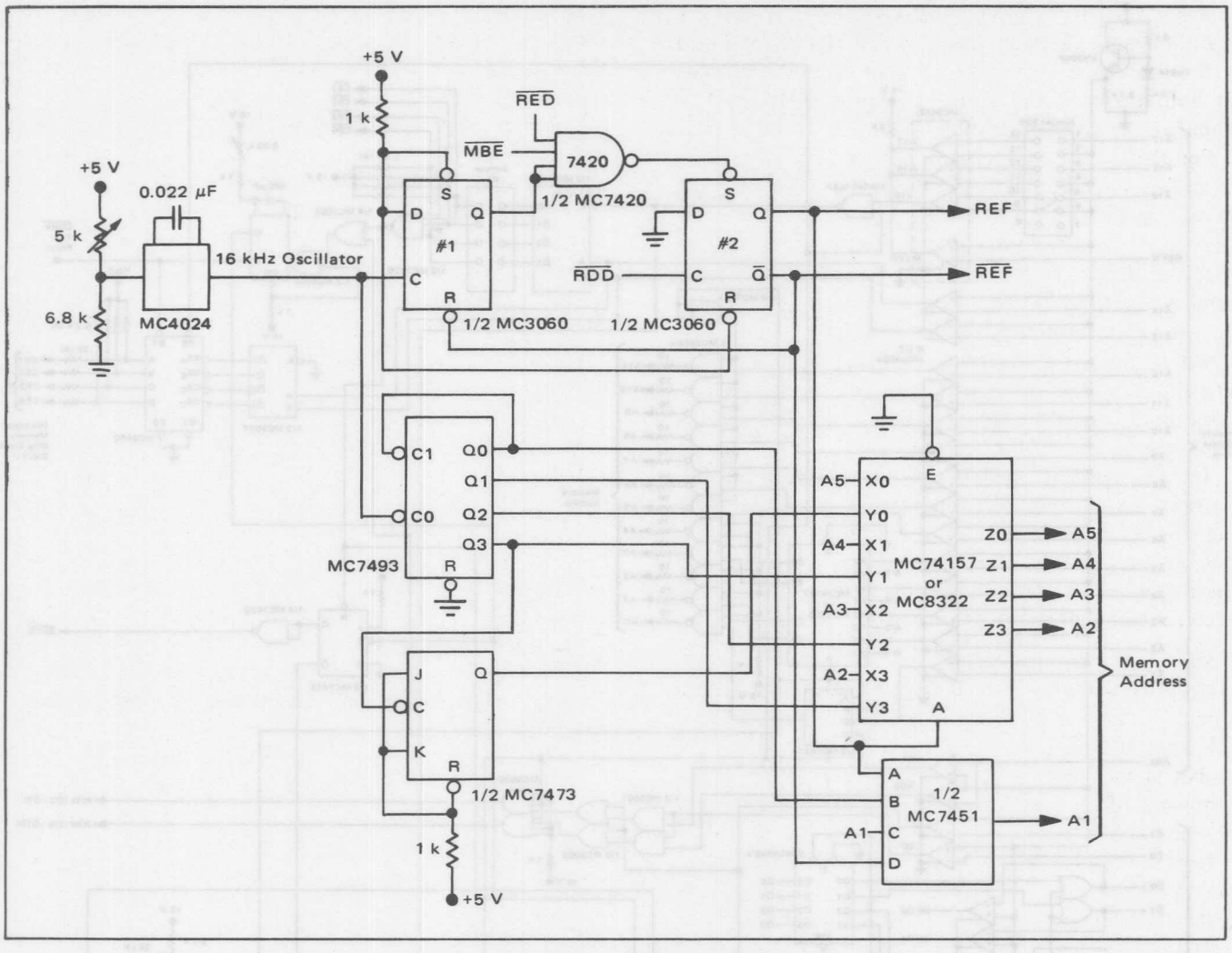


FIGURE 12 – Refresh Address and Refresh Control

a byte as well as a word transfer. Also included in the memory array are address buffers and clock drivers.

The MC3459 Address Line Driver

Although the address inputs of the MCM6605 exhibit low input capacitance (5 pF max), the total parallel input capacitance of these lines in the array can exceed 300 pF. Standard TTL logic gates have insufficient current drive capability to rapidly switch a high capacitive load, therefore, a high speed buffer, such as the MC3459, is required; see Figure 15. The MC3459 has sufficient output current to typically switch a 360 pF load in 20 ns. This fast switching of the lines can cause a considerable amount of overshoot so a 10-ohm series damping resistor is recommended. The output of the MC3459 also has an internal 2.5 k ohm pullup resistor to provide a higher V_{OH} (3.2 V at -640 μA) than standard TTL logic gates. This higher V_{OH} meets the minimum V_{IH} (3.0 V) requirement of the MCM6605.

The MC3460 Clock Driver

The MC3460 quad clock driver, see Figure 16, was employed to meet the high voltage requirements of the memory CE input. The clock driver has internal logic to either select one of the four clock drivers for a normal CPU memory cycle or to select all four drivers at the same time for a refresh cycle. Two enable inputs are also provided for additional memory expansion to 64K words without additional address decoding. Other features of the MC3460 include fast switching (25 ns typical for a 480 pF load), and low dc power for the V_{DD} supply (348 mW max for all four drivers in the logic "0" state).

For the memory array given, each clock driver has to fan out to 16 memory chips. To drive this number of memory chips, an external 6.2 k ohm pullup resistor is required for each driver output to insure a minimum V_{OH} of V_{DD} -1.0 V at a maximum leakage current of 160 μA. A minimum 20 ohm damping resistor is also recommended on the CE lines to reduce overshoot.

The memory system described was laid out on a standard size PDP-11 two-sided PC board as illustrated in Figure 17. A photo of the actual memory board is given in Figure 18.

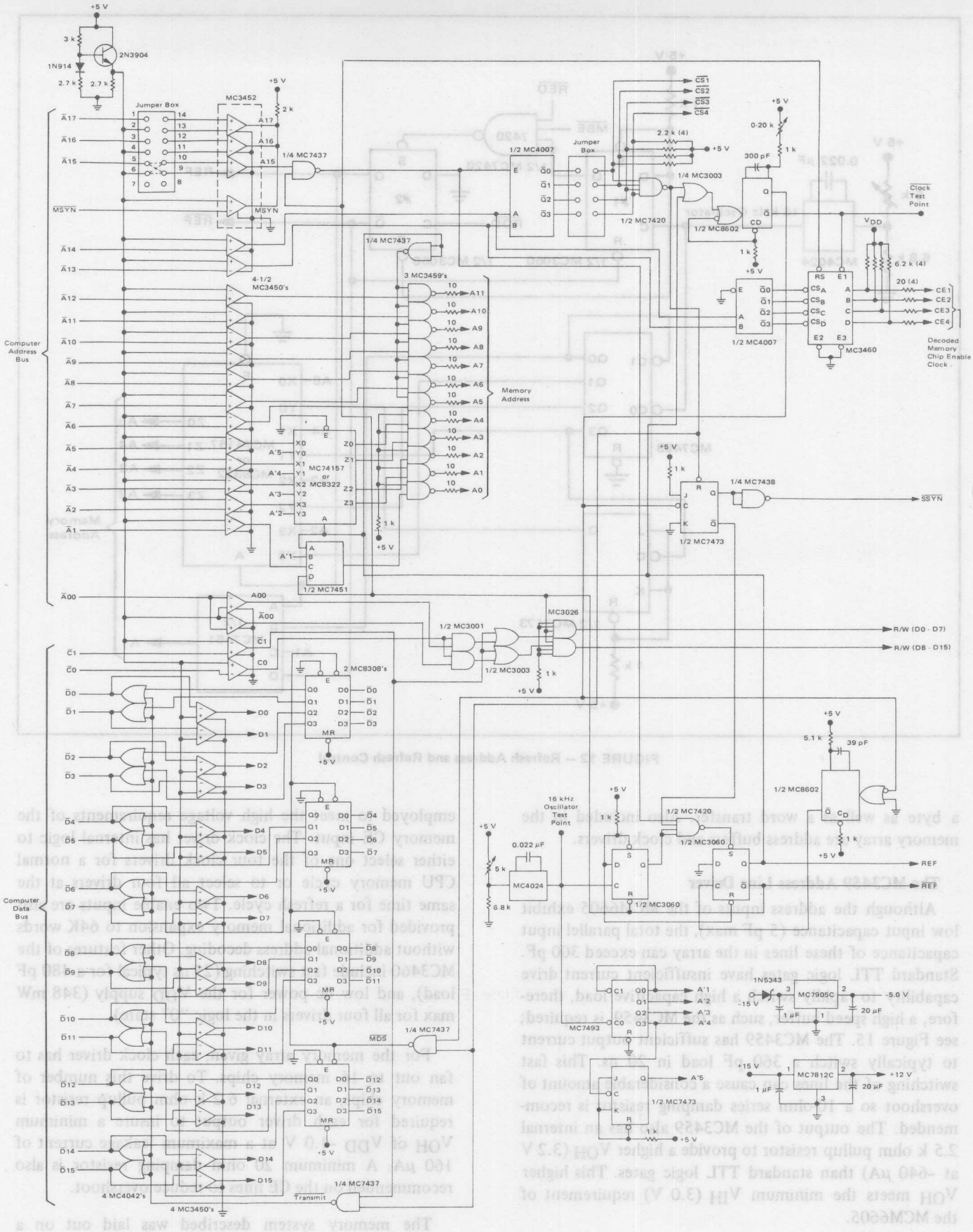


FIGURE 13 – Memory System Schematic

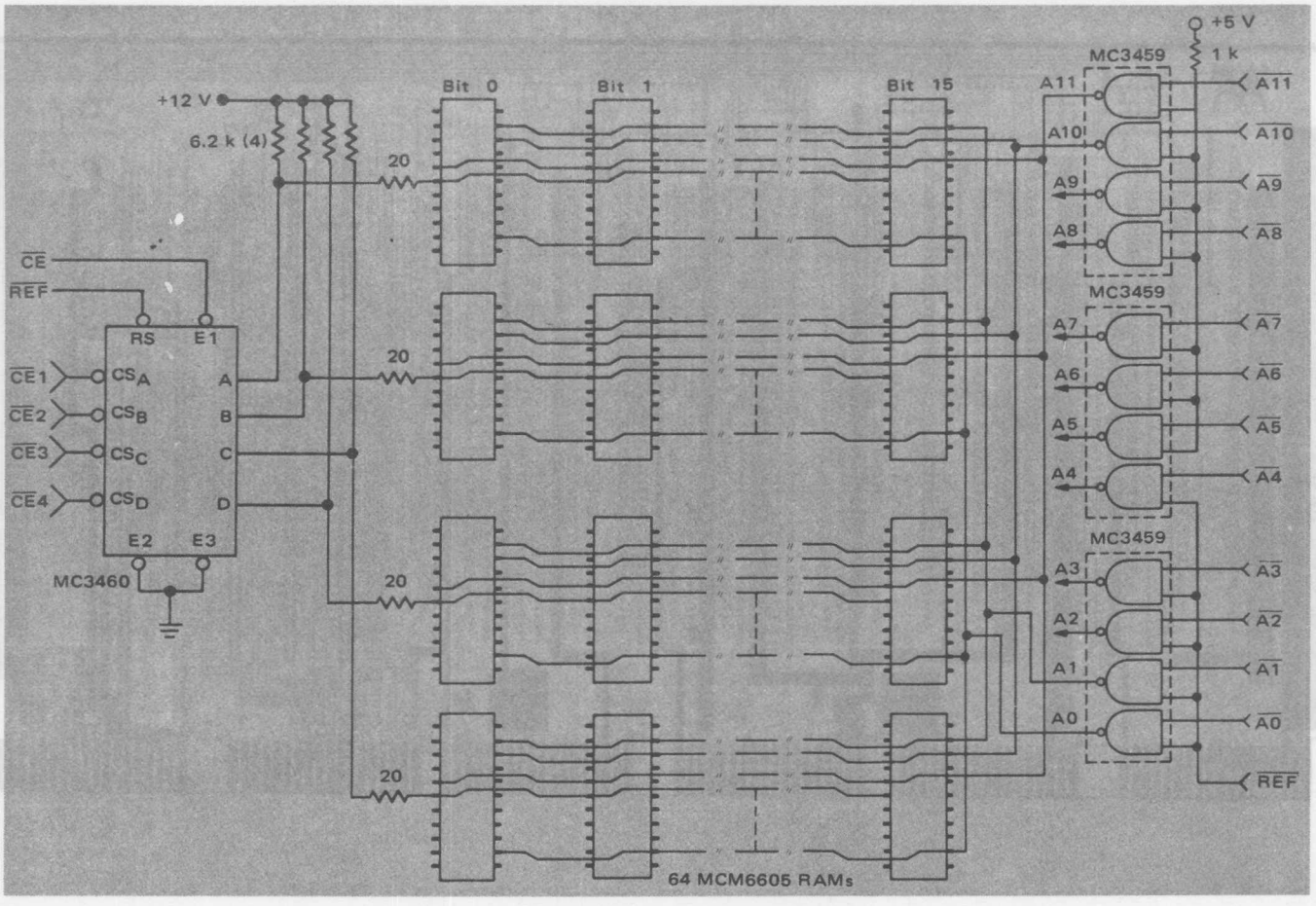


FIGURE 14 – Memory Array

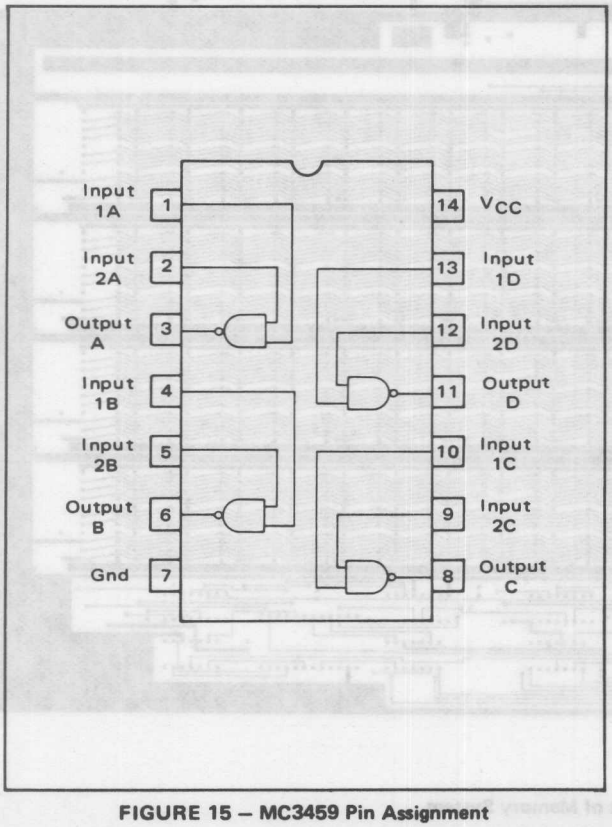


FIGURE 15 – MC3459 Pin Assignment

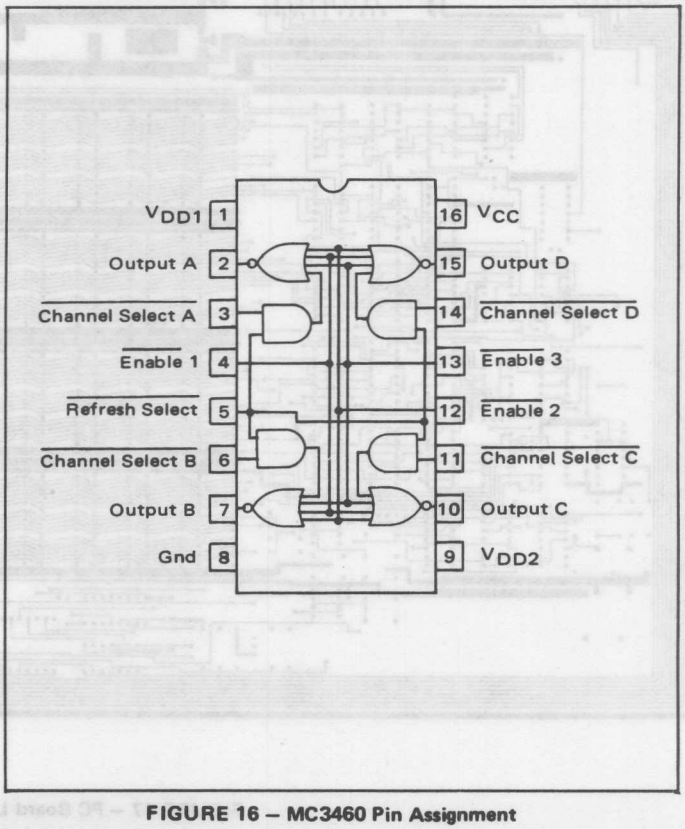


FIGURE 16 – MC3460 Pin Assignment

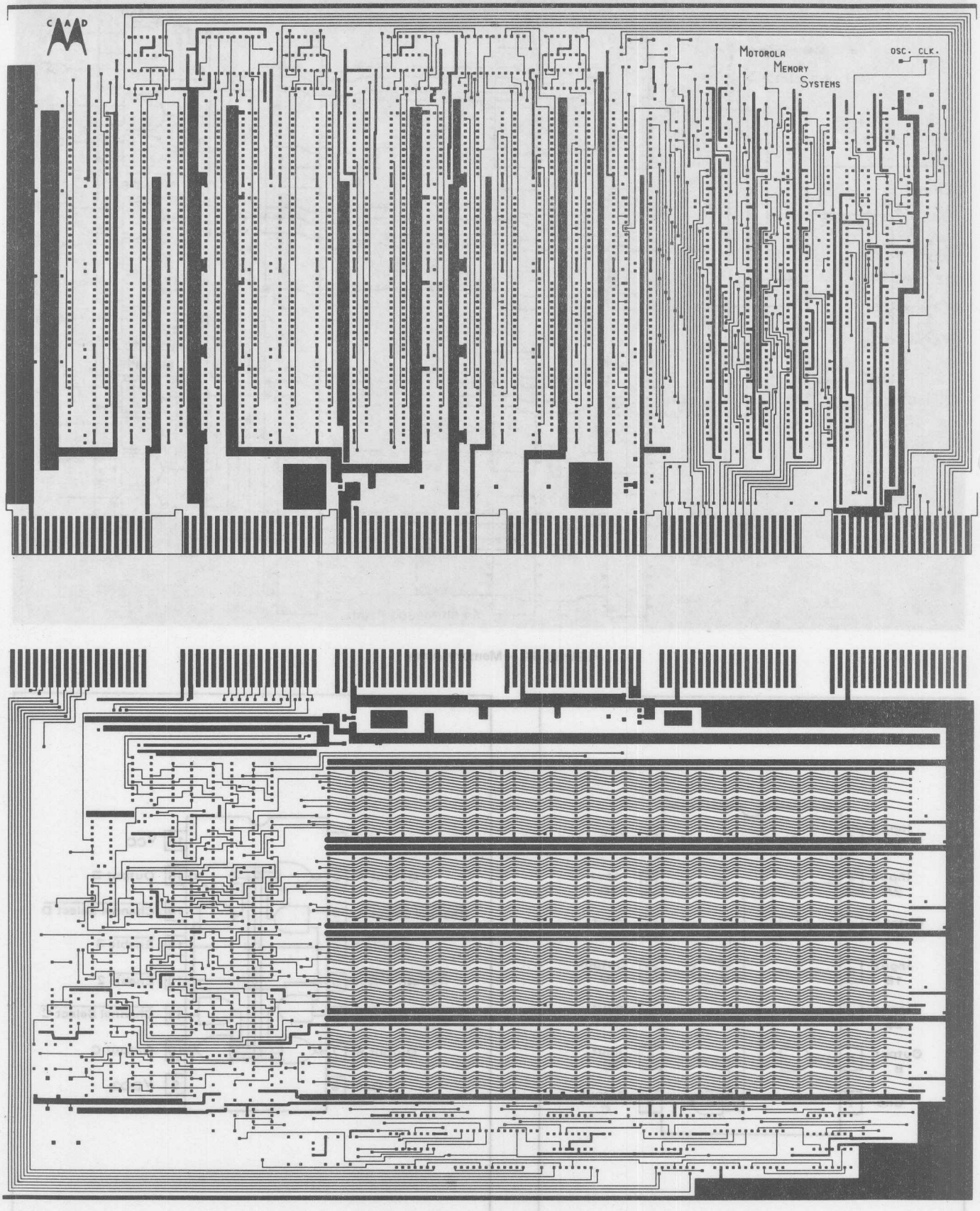


FIGURE 17 – PC Board Layout of Memory System

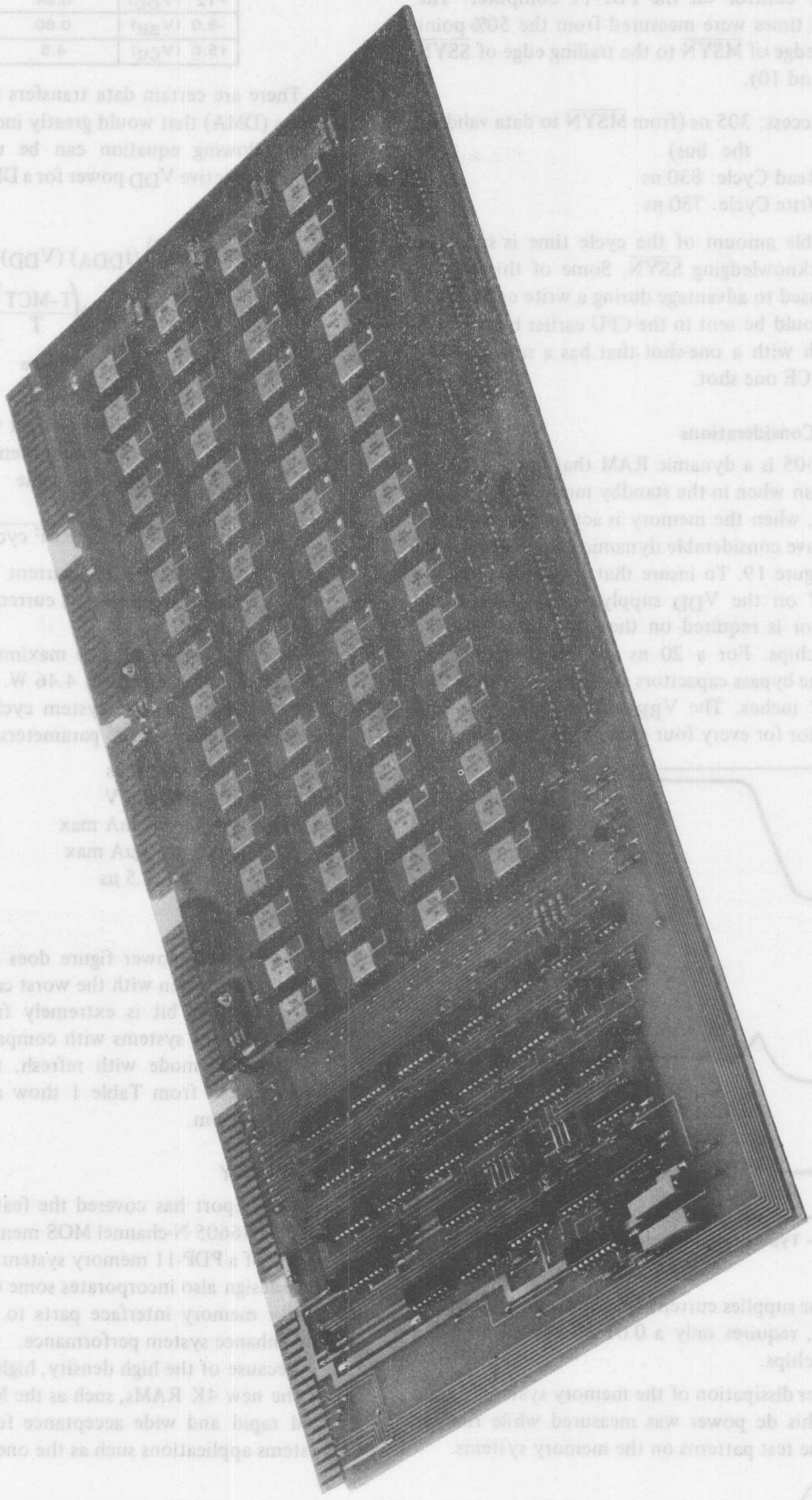


FIGURE 18 – Memory Board

SYSTEM PERFORMANCE

System Access and Cycle Time

The performance of this memory system was measured under program control on the PDP-11 computer. The following cycle times were measured from the 50% point on the leading edge of $\overline{MSYN}$ to the trailing edge of $\overline{SSYN}$ (see Figures 9 and 10).

System Access: 305 ns (from $\overline{MSYN}$ to data valid on the bus)
System Read Cycle: 830 ns
System Write Cycle: 730 ns

A considerable amount of the cycle time is spent by the CPU in acknowledging $\overline{SSYN}$. Some of this wasted time could be used to advantage during a write cycle. That is, the $\overline{SSYN}$ could be sent to the CPU earlier by clocking the $\overline{SSYN}$ latch with a one-shot that has a smaller pulse width than the CE one shot.

System Power Considerations

The MCM6605 is a dynamic RAM that has essentially zero power drain when in the standby mode (CE is a logic "0"). However, when the memory is active, the V_{DD} and V_{BB} supplies have considerable dynamic current transients as noted in Figure 19. To insure that the noise does not exceed 0.35 V on the V_{DD} supply, a low inductance 0.1 μF capacitor is required on the V_{DD} line for every two memory chips. For a 20 ns rise time on the chip enable clock, the bypass capacitors should not be separated more than 1.2 inches. The V_{BB} line requires only one 0.01 μF capacitor for every four memory devices.

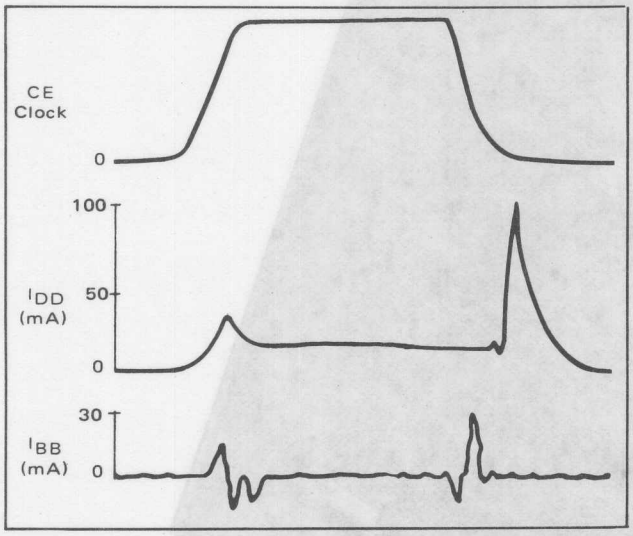


FIGURE 19 – Typical Supply Current Transient Waveforms

The V_{CC} line supplies current only to the output buffer and, therefore, requires only a 0.01 μF bypass for every eight memory chips.

The dc power dissipation of the memory system is given in Table 1. This dc power was measured while running worst-case noise test patterns on the memory systems.

TABLE 1 – Typical Power Requirements for 16K x 16-Bit Memory Board

Power Supply Volts	Standby Power Watts	Active Power Watts
+12 (V_{DD})	0.84	1.10
-5.0 (V_{BB})	0.80	0.80
+5.0 (V_{CC})	4.5	4.75

There are certain data transfers such as direct memory access (DMA) that would greatly increase the V_{DD} power. The following equation can be used to calculate the maximum active V_{DD} power for a DMA type data transfer:

$$P_D = M\left(\frac{MCT}{SCT}\right)(I_{DDA})(V_{DD}) + (N-1)(M) \times \left[\left(\frac{MCT}{T}\right)(I_{DDA})(V_{DD}) + \left(\frac{T-MCT}{T}\right)(I_{DDS})(V_{DD})\right]$$

where: $N = \frac{\text{system word size}}{4096}$

M = number of bits per word
MCT = semiconductor memory cycle time
SCT = system cycle time

$T = \frac{2\text{ ms}}{\text{number of REF cycles}}$

I_{DDA} = active I_{DD} current
I_{DDS} = standby I_{DD} current

Using this equation, the maximum active V_{DD} power for this memory system is 4.46 W. This power figure was determined by using a system cycle time of 830 ns and the following MCM6605 parameters:

(1) MCT = 490 ns
(2) V_{DD} = 12.6 V
(3) I_{DDA} = 36 mA max
(4) I_{DDS} = 20 μA max
(5) T = 62.5 μs

The calculated power figure does not include the clock driver power. Even with the worst case DMA power figure, the power per bit is extremely favorable compared to other memory systems with comparable performance. In the standby mode with refresh, the average dc pow figures taken from Table 1 show a typical 23.4 μW/bit for this system.

SUMMARY

This report has covered the features and operation of the MCM6605 N-channel MOS memory, and the complete design of a PDP-11 memory system employing this device. This design also incorporates some of the newest semiconductor memory interface parts to reduce package count and enhance system performance.

Because of the high density, high speed, and low power of the new 4K RAMs, such as the MCM6605, they should find rapid and wide acceptance for mainframe memory systems applications such as the one just covered.

MOTOROLA Semiconductor Products Inc.

Printed in Switzerland

AN-740